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14. ABSTRACT

A 4Mbit non-volatile Chalcogenide-Random Access Memory (C-RAM™) has been designed and fabricated in RH25, a radiation hardened CMOS technology. The top-down design focused on accommodating chalcogenide process variations and satisfying space system specifications. The optimized band-gap circuit supplies reference current and voltage that meet temperature and voltage requirements. The innovative write circuitry supplies appropriate currents (amplitude and shape) to the chalcogenide memory cells to allow them to be programmed either in amorphous state (write "0") or crystalline state (write "1"). The on-chip pulse generator circuit can provide multiple pulse widths for write "0" and write "1", as well as preconditioning pulse. The write circuits have a dedicated power supply, which can be removed to place the part in a read only mode. The read circuitry includes a voltage limiting circuity, an adjustable current reference, an adjustable pre-charge circuitry, and a sense amplifier to accurately sense the current difference between cells programmed as "0" or "1". A localized redundant cell architecture is implemented with shared read/write circuits to improve yield without impacting access times. The redundant cells can be tested prior to laser fusing or used to monitor endurance. Considerations for testability such as direct chalcogenide cell access, margin test, analog monitors, and endurance acceleration have been implemented. Noise and power reduction techniques have also been used globally.

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A 4-Mbit Non-Volatile Chalcogenide-Random Access Memory Designed for Space Applications

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Abstract-- A 4Mbit non-volatile Chalcogenide-Random Access Memory (C-RAM™) has been designed and fabricated in RH25, a radiation hardened CMOS technology. The top-down design focused on accommodating chalcogenide process variations and satisfying space system specifications. The optimized band-gap circuit supplies reference current and voltage that meet temperature and voltage requirements. The innovative write circuitry supplies appropriate currents (amplitude and shape) to the chalcogenide memory cells to allow them to be programmed either in amorphous state (write "0") or crystalline state (write "1"). The on-chip pulse generator circuit can provide multiple pulse widths for write "0" and write "1", as well as a pre-conditioning pulse. The write circuits have a dedicated power supply, which can be removed to place the part in a read only mode. The read circuitry includes a voltage limiting circuit, an adjustable current reference, an adjustable pre-charge circuit, and a sense amplifier to accurately sense the current difference between cells programmed as "0" or "1". A localized redundant cell architecture is implemented with shared read/write circuits to improve yield without impacting access times. The redundant cells can be tested prior to laser fusing or used to monitor endurance. Considerations for testability such as direct chalcogenide cell access, margin testing, analog monitors, and endurance acceleration have been implemented. Noise and power reduction techniques have also been used globally.

***Index Terms*—Chalcogenide, phase change, nonvolatile, memory**

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I. INTRODUCTION

A phase change chalcogenide memory has been considered in the aerospace community as the future non-volatile memory for space applications. BAE Systems and Ovonyx, under contract to the Space Vehicles Directorate of the Air Force Research Laboratory (AFRL) since 1999, have been working on research and development of Chalcogenide Random Access Memory (C-RAM). The C-RAM program integrates the phase-change technology into a radiation hardened CMOS process developing a radiation-hardened, fast, low-power, high-endurance non-volatile memory. The resulting device can work in extreme radiation environments (total ionizing dose and single event effects) with the capability of retaining data for years and cycling thousand of times per day through the life of a system. A 4Mbit prototype chip has been designed and fabricated in RH25, a 250nm radiation hardened CMOS technology. The design was completed concurrently with process development.

In this paper, we present the variety of test modes, trim pins, and unique circuits that were developed to accommodate material requirements, process variation, and potential future process enhancements. The architecture is described in section II. The techniques we used for compensation and noise reduction are discussed in section III. Read and write circuits are presented in section IV and section V respectively. Section VI explains the design validation, and finally, we summarize in section VII.

II. ARCHITECTURE & FEATURE OVERVIEW

The architecture of the 4 Mbit C-RAM is shown in Figure 1. It consists of eight memory blocks and a center control section. Each block is comprised of a 512Kbit memory array that is partitioned into 8 sub-block pairs, each of which contains 256 rows and 256 columns of memory cells, resulting in a 64Kbit array as the minimum sized building block.

Extra redundant rows and columns are embedded locally at the sub-block level. These redundant rows and columns utilize the existing read and write circuitry and cause no

degradation in performance. If a defective cell is located during testing, fusing can be performed to swap in one of the available redundant rows or columns. All redundant rows and columns can be tested prior to fusing to guarantee their viability. An additional benefit of the redundant cell test mode is the ability to perform destructive testing on unused redundant rows or columns without damaging the cells that are used in the final product. This could, for example, allow cycling of unused redundant cells to the point of failure on each die to facilitate endurance characterization.

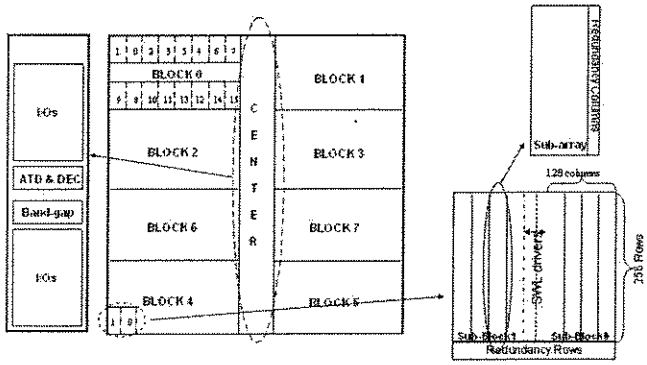


Figure 1 4Mbit C-RAM Architecture

With only one metal mask change, the architecture can be converted from 4Mbit (512k x 8) to 2Mbit (256k x 8). During a read, a low voltage is applied across the memory cell and a current is measured. For 4Mbit operation, the sense amplifier compares the current flowing through each chalcogenide cell to an internally generated reference current. For 2Mbit operation, pairs of cells are written to opposite polarities, and during a read, the currents of the two cells are compared directly. The 2Mbit option carries a large penalty for density, but, as shown in Figure 2, provides additional margin during read.

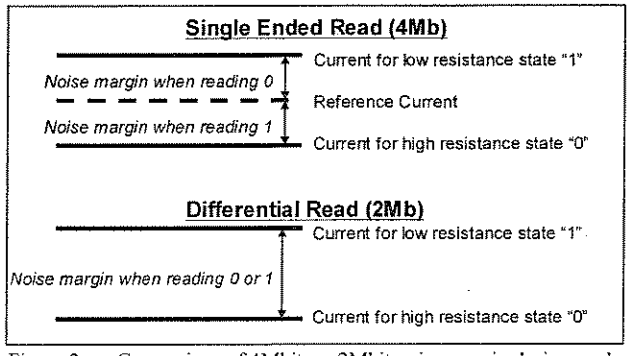


Figure 2 Comparison of 4Mbit vs. 2Mbit noise margin during read

The center control section is composed of Input/Output (I/Os) circuits, an address transition detection (ATD) circuit, address decoders, and a band-gap based compensation circuit. The centralized I/Os provide balanced data out paths, and a staggering technique used to enable the off chip drivers (OCDs) that significantly reduces switching noise. The ATD circuit supplies an internal clock for the read and write circuits and has a programmable fuse feature for timing optimization. The band-gap's function is to generate a voltage and temperature compensated current source with high noise rejection. This current is distributed throughout the chip and has an important role in both the read and the write circuitry. For the read circuitry, the current source provides the foundation for the sense amp reference current generator, the voltage limiting circuit (VLIMIT), and the pre-charge circuit. For the write circuitry, the current source compensates the write current and controls the write pulse width in the pulse shaping circuit.

Other features embedded in the design include various trim controls to fine tune the circuits for process variation, and a number of test modes to allow full characterization of the design and each of the memory cells. All of the trim settings can be varied during test to find the optimal operating conditions. Once this operating point is determined, the settings are locked in with laser fusing. The settings that can be adjusted are: band-gap current selection, band-gap temperature response, write "0" pulse width, write "1" pulse width, write current amplitude, sense amp reference current (switching point), and pre-charge voltage level. The test modes available include memory cell margin test, endurance acceleration mode, single pulse forming (SPF) mode, band-gap override, and redundant cell test mode. This architecture also introduces an analog read technique that provides a powerful tool for chalcogenide cell characterization.

These trim and test mode selections offer the valuable capability to accommodate different chalcogenide alloys over a wide voltage and temperature range, to reliably characterize cell endurance and margin, and to provide for process variation from chip to chip, wafer to wafer, and lot to lot.

III. Compensation & Noise Reduction

A. *Band-gap Current Compensation*

In the 4Mbit C-RAM band-gap implementation, shown in Figure 3, the current source amplitude and slope across temperature is defined by the transistor sizes, the diode characteristics, and the resistor parametrics. For such a key circuit, it is imperative to ensure that the actual hardware output current is well matched to its simulation counterpart. To help mitigate effects from variation in poly sheet resistance, the diode characteristics, and the transistor gain, selectable resistors were implemented in the design to tune the current slope across temperature. At the output of the band-gap, a current mirror bank was added in-line to compensate for variations in the current magnitude. With these additional

controls, the band-gap design now can produce a known, compensated current despite some variation in process.

To test the band-gap, two test options are also provided on the chip. The first option uses the analog read circuitry that is integrated into every sense amplifier in the design to measure the sense amplifier reference current. The band-gap output is distributed through a series of low error current mirror structures to the sense amplifier reference circuit. This provides a current path from the band-gap output to the analog read output that can be measured with analog probes. Using analog read is the best tool to obtain data about the band-gap current magnitude and slope across temperature.

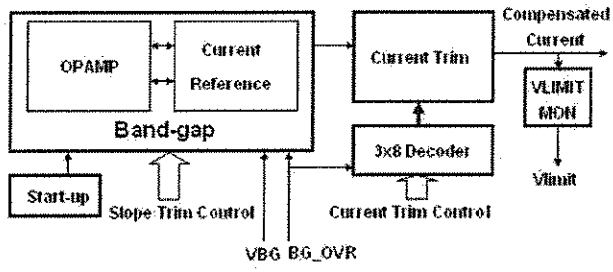


Figure 3 Band-gap and current trim

An alternate option is to measure the voltage from the VLIMIT circuit. A portion of the current distribution network was duplicated and connected to an additional VLIMIT circuit near the band-gap. This voltage limiting circuit can be measured through a test pin on the chip and compared to a known value. At test, this can provide an easy way to indirectly measure the band-gap magnitude since the output voltage of the voltage limit circuit is mathematically related to the band-gap current amplitude.

Based on the results from either band-gap test option, the band-gap circuit can be tuned to match the desired current magnitude and slope across temperature. If the band-gap current is beyond the tuning range, then to promote testability of other structures in the chip, a band-gap override switch was designed into the final current switch bank. This allows the user to override the band-gap to any desired current. If further testing of the band-gap circuit is desired, a stand-alone circuit is also available.

B. *Noise Reduction*

All read and write circuits in the 4Mbit C-RAM design utilize the compensated current from the band-gap reference. As the current is distributed, the current levels are kept small to minimize power consumption and guarantee accurate mirroring without losing supply voltage and temperature compensation. When the distributed source current arrives at the read or write circuits, it is converted into reference voltages, some of which are marginally above the threshold voltage of the transistors. Operating with voltages in this range means that switching noise could easily disturb the reference levels. In addition, once perturbed, these voltages would require an unacceptable recovery time due to the low current amplitudes. Therefore, a number of measures were taken to stabilize all reference voltages. First, to reduce noise from the power supply, all analog circuits in the design were connected to a separate power distribution network with localized on-chip decoupling capacitors. Also, as the reference current is mirrored across the chip, capacitors are used to maintain a constant Vgs for all transistors in the distribution path, as seen in Figure 4. The metal lines used to distribute these analog currents and voltages were placed in dedicated wiring tracks with sufficient spacing laterally and vertically to prevent undesired coupling. Wherever possible, additional shielding layers were added to further isolate the analog signals in the design.

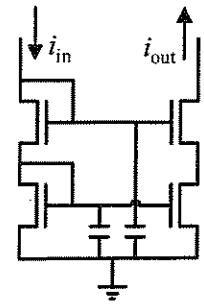


Figure 4 Reference voltage stabilization in current mirrors

In addition to isolating and stabilizing the analog components of the design, great care was taken to minimize the noise generated in the digital circuits. Design segmentation was used extensively through address decoding to gate off all control signals, generated clocks, and write pulses from switching in inactive areas of the chip. Any gates that were not located in the critical timing path were designed to switch slowly to minimize the peak current drawn by the digital logic.

IV. Read Circuitry

A. *Sense Amplifier Reference Current and Pre-charge*

Figure 5 shows the circuitry that generates the sense amplifier reference current, determines the pre-charging voltage level, and creates an analog sense reference override signal. The sense amplifier reference circuit provides a range of reference currents for reading the resistance of the chalcogenide cell. The design was implemented with high noise rejection by using capacitors and cascoded current mirror structures. The chalcogenide material has a distribution of set and reset resistance values that may vary from chip to chip or with future process changes. Multiple switches allow for programming the sense amplifier reference to the desired current for a given distribution. Maximizing the difference in the reference and the actual cell current increases the noise

margin and reduces the read time. As each current level is selected, the precharge voltage is adjusted to provide optimal performance.

One main feature of the sense amplifier reference circuit is the analog reference override (AREF). This override allows test of the sense amplifier and the cell resistance above and below the built-in reference range to determine margin in programmed bits. Bits with lower margin can be, if desired, marked and swapped with the available built-in redundancy. AREF, an external control signal, is grounded to disable the override in normal operation, and shmooed in the range that is greater than a specified $V_{override}$, during margin test. The threshold of $V_{override}$ provides noise margin in case of noise on the override input. In short, this analog reference override allows measurement of sets and resets across the 4Mbit array quickly since it uses the sense amplifier and digital output path and no analog measurements are necessary.

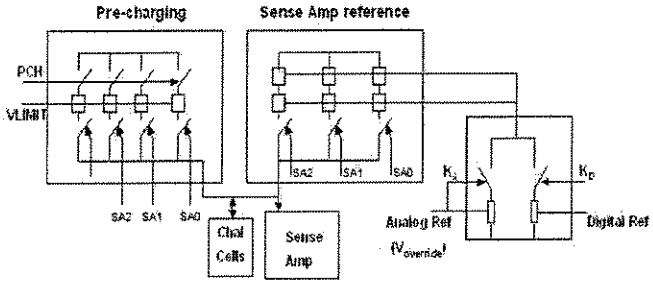


Figure 5 Sense set points and pre-charging

B. *Analog Read Circuitry*

Direct chalcogenide cell access to all 4Mbits is available in addition to AREF margin testing as a slower, but more accurate tool. This powerful capability can be used to generate exact cell resistance distributions. The analog read circuitry is embedded in each sense amplifier throughout the chip and is enabled through a combination of an enable pin and the read column select signal. This implementation shares the same decoding logic with the digital circuitry and allows the resistance of eight cells to be measured in parallel. In analog read mode, all internal current paths into the cell are shut off allowing an accurate current measurement after a small external voltage is applied. To maintain full analog read capability for the 2Mb differential version of the design, an additional control signal determines whether the cell connected to the true side or the complement side of the sense amplifier is selected.

Another valuable feature of the analog read circuitry is the ability to measure the sense amplifier reference currents. This measurement is achieved by measuring the complement input of the sense amplifier in the 4Mbit single ended version of the design. By stepping through the address space, the current distribution across the chip can be monitored by comparing each of the sense amplifier reference currents. In addition, an accurate value of the reference currents allows the calibration of the override AREF option, since it allows the user to compare the normal operating current from the sense amplifier reference with the current obtained by varying $V_{override}$.

C. *Voltage Limiting Circuit*

Another key component in cell reading is the voltage limiting circuit. This circuit compensates an NMOS transistor threshold across temperature so that the voltage across the chalcogenide cell remains both constant and below the read disturb limit. A duplicate voltage limiting circuit was placed near the band-gap and provided with a pad for analog measurement of voltage limiting circuit during test. While this component contains the least amount of user control of all the read circuits, it does have one control that works in conjunction with the analog read capability. In analog read mode, a switch forces the voltage output to the rail. This removes voltage limiting on the NMOS access transistor in-line with the cell and allows accurate analog measurement.

V. Write Circuitry

A. *Chalcogenide memory characteristics*

Figure 6 shows the chalcogenide memory cell I-V characteristic curve. The high resistance amorphous material shows very little current below a threshold voltage of V_T while the low resistance polycrystalline material shows a significantly higher current in same region. When applying voltage above V_T, both polycrystalline and amorphous display identical I-V characteristics, with a dynamic resistance ($R_{DYNAMIC}$) of $\approx 1k\Omega$.

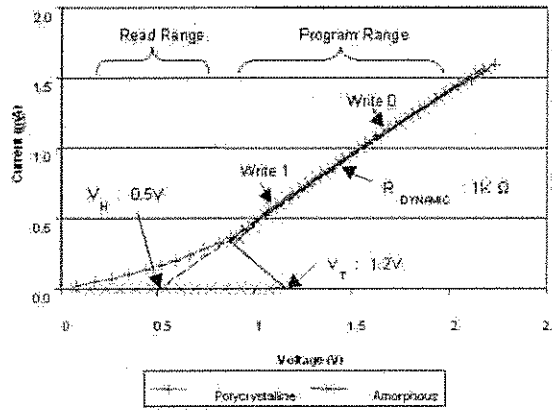


Figure 6 I-V Characteristic of chalcogenide memory

In the program range, the chalcogenide memory can be programmed to either low resistance state (write "1") or high resistance state (write "0") by providing different write current amplitudes to heat the material to either polycrystalline state or amorphous state, as shown in Figure 7. Writing a "1" requires lower current and with a long cooling time, while writing a "0" requires higher current and much quicker

cooling time. Extrapolation of the portion of the I-V curve that is above V_T to the X-axis yields a point referred to as a holding voltage (V_H). The applied voltage must be reduced below V_H to exit the programming mode. The state of the memory cell is read using the difference in I-V characteristics below V_T.

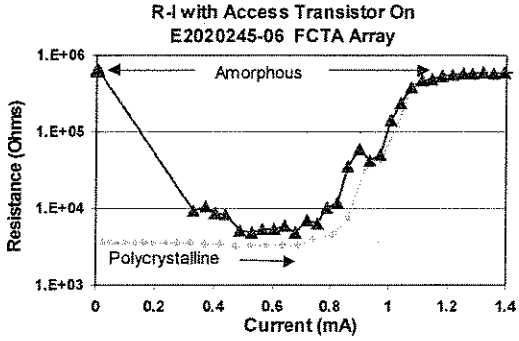
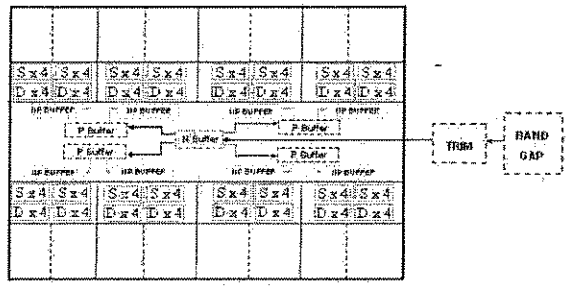
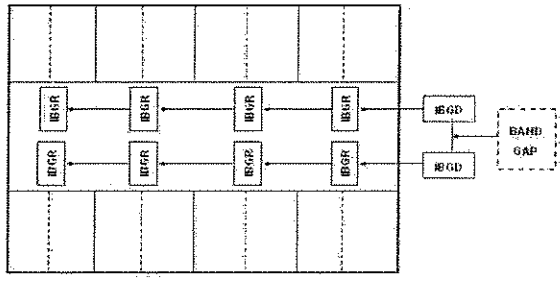


Figure 7 R-I Curve of chalcogenide memory

B. *Current Distribution*



(a) Write Current Distribution



(b) Read Current Distribution

Figure 8 Write and read current distributions

To distribute the compensated band-gap current, a fully symmetric current distribution network was set up across the chip. The block diagrams in Figures 8a and 8b show the current network inside of a 512Kbits block. In conjunction with the band-gap, the network can evenly distribute the current to each sub-array without interruption from noise or loss of compensation. The accurate distribution of read current is important to guarantee that all cells are being compared to the same reference current across the chip. The accurate distribution of write current with the correct amplitude is also critical to insure uniform programming of bits across the array. The read and write current networks are separated in the design to allow independent trim controls and to prevent coupling noise from one operation to the other. Also, the write network operates with higher current amplitude than the read network, so an H tree design was adopted to match IR-drop across the 512K block. As mentioned previously, the analog read circuitry can provide insight into the accuracy of the current distribution across the chip.

C. *Write Current Amplitude*

Because of the importance of write current amplitude, a variety of control options are provided. Figure 9 shows the all of the controls that are available to manipulate the write current amplitude. Both the band-gap and current trim circuits are located at center of the chip while current buffers are arranged evenly inside of the block. A well compensated current from the band-gap circuit feeds to current buffers, which distribute the current to the write head circuits.

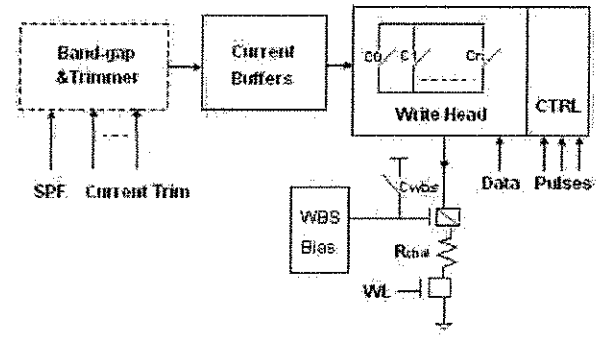
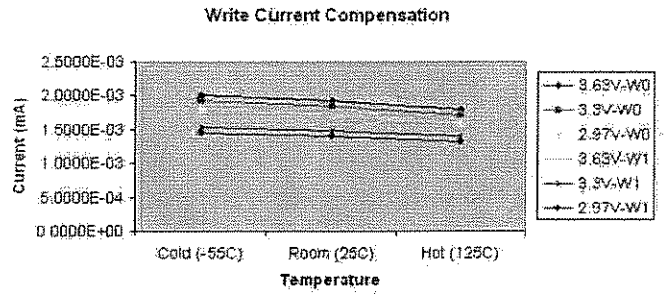
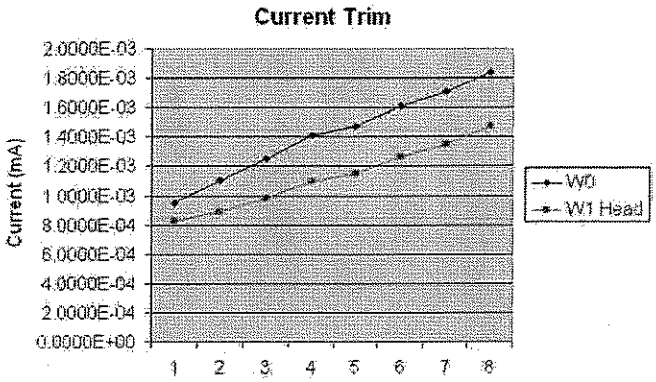


Figure 9 Write circuitry

A write head consists of switches C_0 through C_n and related control circuits. It is shared by a 32 x 256 array referred to as a data bit. By controlling how many of the switches are on, the amplification of the band-gap current is modulated, allowing the write head to supply the appropriate write "0" current or a lower amplitude shaped write "1" current. Cascoded devices were used in the current buffers as well as the write head circuits to achieve better compensation. Also, a write bit switch bias circuit was used to keep the column select transistor in saturation. The currents applied to the chalcogenide memory cell are compensated with a desired modulation across temperature and supply voltage over the full military specification as shown in Figure 10.



(a) Compensation



(b) Current trim

Figure 10 Write current compensation and trim

Finally, a separate power supply (VPP), is connected to the write current buffers and write head circuits. If the VPP supply is driven to ground, the chip enters a failsafe read-only mode where performing a write is prohibited due to absence of high current through the cells. Therefore, in addition to having logical write protection from the external control signal WPN, an isolated VPP for the write circuit provides definite write protection that is desired by space and military applications.

D. *Pulse Width, Shape, & Endurance Acceleration*

Along with the current amplitude, the shape and width of the write current pulses are also very important to create well programmed set and resets. The write pulse generator circuit, as shown in Figure 12, provides flexibility in the write current pulse width with externally accessible pads. It can generate eight different write "1" pulses ranging from 250ns to 12.8us (for forming pulse, if needed) and two different write "0" pulses to cover process variability and future chalcogenide alloy enhancements. This was implemented with a variable write pulse generator that has a selectable loop length. For each write cycle, the circuitry generates a write "0" pulse, a write "1" pulse, and four clocks that are used to shape the write "1" current forced through the memory cell.

Also, a single pulse forming (SPF) mode provides a much longer, higher amplitude write "1" pulse that can be used to precondition the chalcogenide material of each memory cells. A final option allows a user defined pulse width for writing "0" that can override the internal reset pulse width. The user override feature can be implemented in conjunction with maximum write current amplitude to allow accelerated endurance testing.

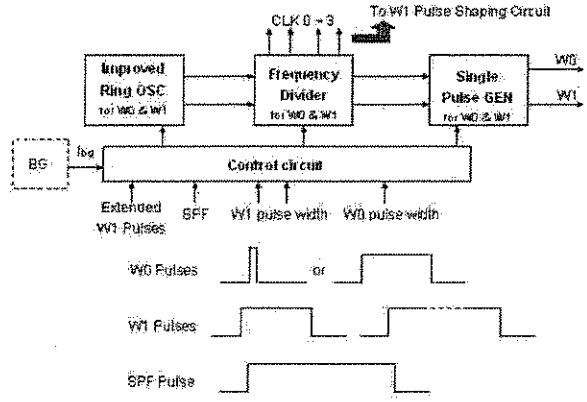


Figure 11 Write pulse generation circuits

During device test, the design flexibility allows the test engineer the ability to find the settings with the best distribution of sets and resets. With future process improvements, the design has the ability to be set to shorter write times for set and reset pulses without redesign.

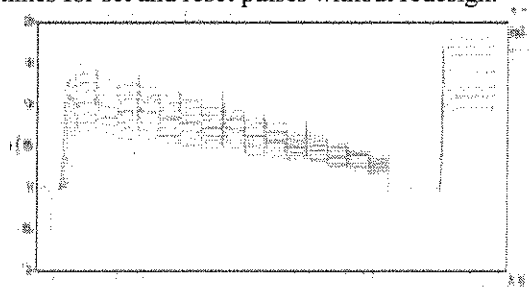


Figure 12 Write current pulse shaping

VI. Design Validation

The 4Mbit C-RAM design has been validated at both wafer and module level. The first step of wafer level validation includes calibrating each individual die using the trim provided in the design. The calibration begins with determining the correct trim setting for the band-gap to offset poly sheet resistance variation. This was completed by measuring the central VLIMIT circuit output voltage and adjusting the resistor trim for the band-gap until the expected output was matched.

After collecting initial programmed set and reset resistances using the sense amplifier reference trim, the best write amplitude trim setting was selected by adjusting the write amplitude trim to produce the optimum result from a programmed checkerboard of 1's and 0's at a specified sense amplifier reference trim and initial write pulse width. Next,

the write "0" pulse width trim was adjusted, and the amplitude trim was again cycled. The best combination of write amplitude and pulse width (highest margin) for each die was then selected.

Several selected die have been packaged into either 40 pin product modules or 256 pin test and characterization modules for module level testing. The 256 pin test and characterization module provides access to all trim and measurement features to facilitate margin test, debug, and characterization over temperature. A more exhaustive tuning methodology is in development to provide valuable statistical data and increased margin.

Other test controls have been verified as functionally working such as AREF, write pulse width override, and analog read. Analog read, in particular, has been a very useful tool. The analog read circuit has been used to measure the cell resistance and the sense amplifier reference current to provide insight on design and process characteristics.

VII. Summary

During this stage of a multi-year research program, BAE SYSTEMS and Ovonyx have begun validation and characterization testing of a 4Mb non volatile chalcogenide random access memory (C-RAM) device. Characterization of the first pass design of the 4M C-RAM is complete and Pass 1 results were factored into the final Pass 2 design. Several lots have been fabricated with some wafers having fully functional die. Design features that provide a variety of test modes, circuit performance trims, and measurement capabilities are facilitating the required characterization of the chalcogenide technology. In addition, the fully symmetric architecture ensures the uniformity necessary for optimum read and write performance across the 4Mbit array. Significant design flexibility has been incorporated to accommodate process variation and future process changes. The first lot of 4M C-RAM second pass devices have been received and initial testing shows that the design supports voltage and temperature requirements for space applications. Radiation testing is ongoing.

VIII. Acknowledgements

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